Die Products

Die - The Ultimate Small Form Factor Package

Today, designers face the challenge of incorporating more functionality into a limited space in both a timely and cost effective manner. For many portable and small form factor applications, silicon packaging has become the major size-limiting element of the design layout. Here, the conversion from standard semiconductor packaging to unpackaged die provides designers with a more efficient use of the limited substrate space. Die products provide the ultimate opportunity for size and weight reduction, electrical performance improvements, enhanced function integration and reduced costs in system design.

COB Applications

Converting surface mount package designs to either chip-on-board (COB) or flip chip can result in a 50% to 75% footprint layout reduction utilizing the same functional device design.

Die for chip-on-board (COB) wire bond applications

The COB die implementation utilizes our standard bond pad metalization and die surface passivation. The interconnects are located on the periphery of the device. Interconnect methods for COB wire-bonding include gold-ball bonding and aluminum wedge bonding.

The Benefits of Die

Electrical Performance

The lower inductance and capacitance of the unpackaged die is important in analog, RF and power applications. Improvements are also made to signal propagation and power/ground distributions.

Size and Weight

The improvement in size and weight with the use of unpackaged die will vary based on the current package outline employed. Unpackaged die can also reduce the height of the overall solution.

Reliability

The reduced number of interconnects between active silicon and the substrate with die use leads to improved reliability. A typical package has three connection points vs. two for wire bonds and a single joint with flip chip.

Improved integration

Using existing silicon functions can provide a low-cost, low-risk path for designers to realize higher levels of integration without relying on more extravagant system-on-chip (SOC) solutions. By taking advantage of existing unpackaged die products and high-density substrates to create system-in-package (SiP) solutions, designers can also significantly reduce their design time.

The National Advantage

National Semiconductor offers a wide range of die products and the support information required to take advantage of this technology

- Die specific datasheets
- Samples
- Technical support
- Extended temperature range guarantees
- Shipping/delivery options for both wafer and die including wafer on film-frame, gel paks, waffle packs or tape and reel.

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